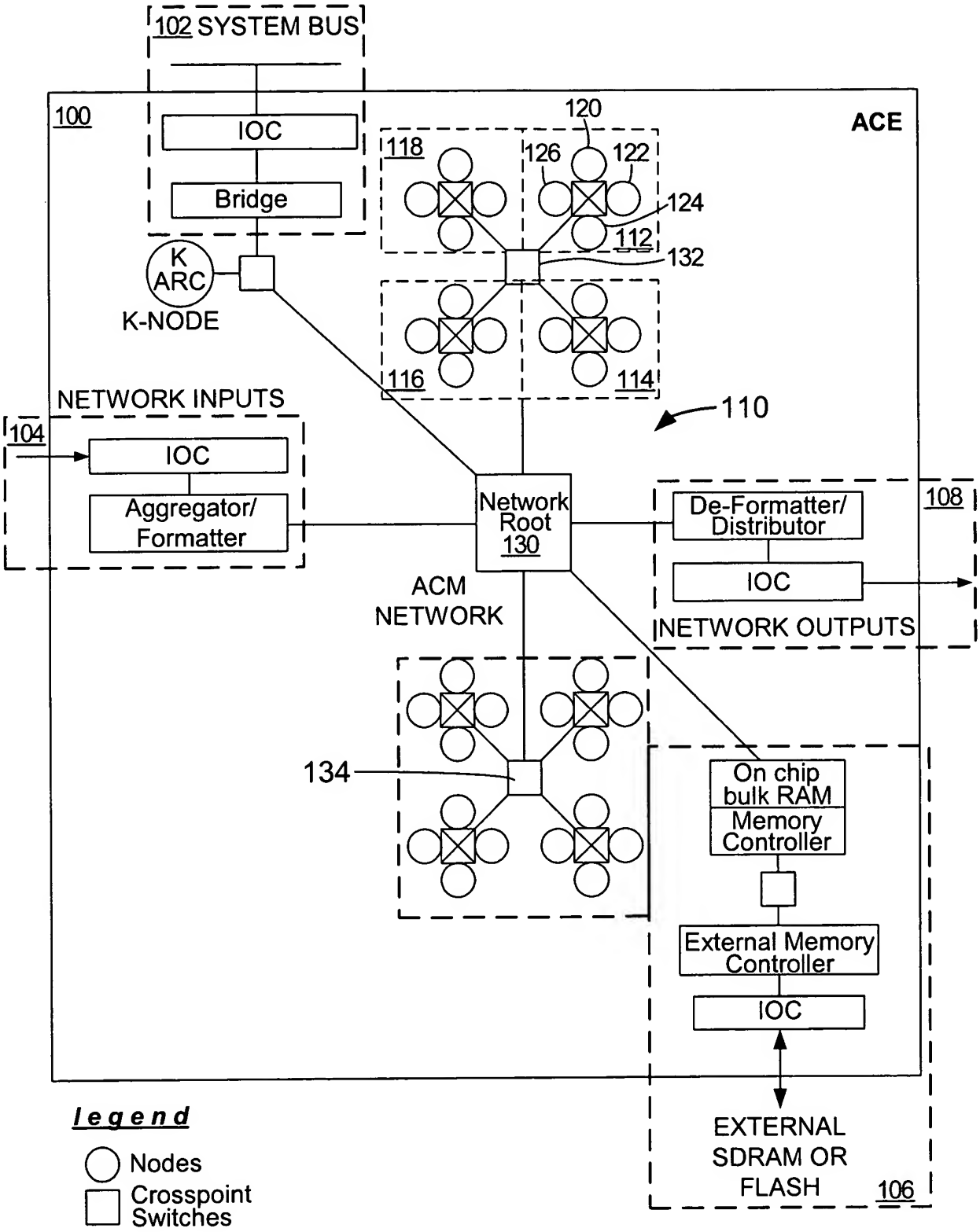
102 SYSTEM BUS
100
IOC
Bridge
K
ARC
K-NODE
120
118
126
122
124
112
132
116
114
ACE
110
NETWORK INPUTS
104
IOC
Aggregator/
Formatter
Network
Root
130
ACM
NETWORK
De-Formatter/
Distributor
IOC
108
NETWORK OUTPUTS
134
On chip
bulk RAM
Memory
Controller
External Memory
Controller
IOC
EXTERNAL
SDRAM OR
FLASH
106
Legend
Nodes
Crosspoint
Switches

FIG. 1

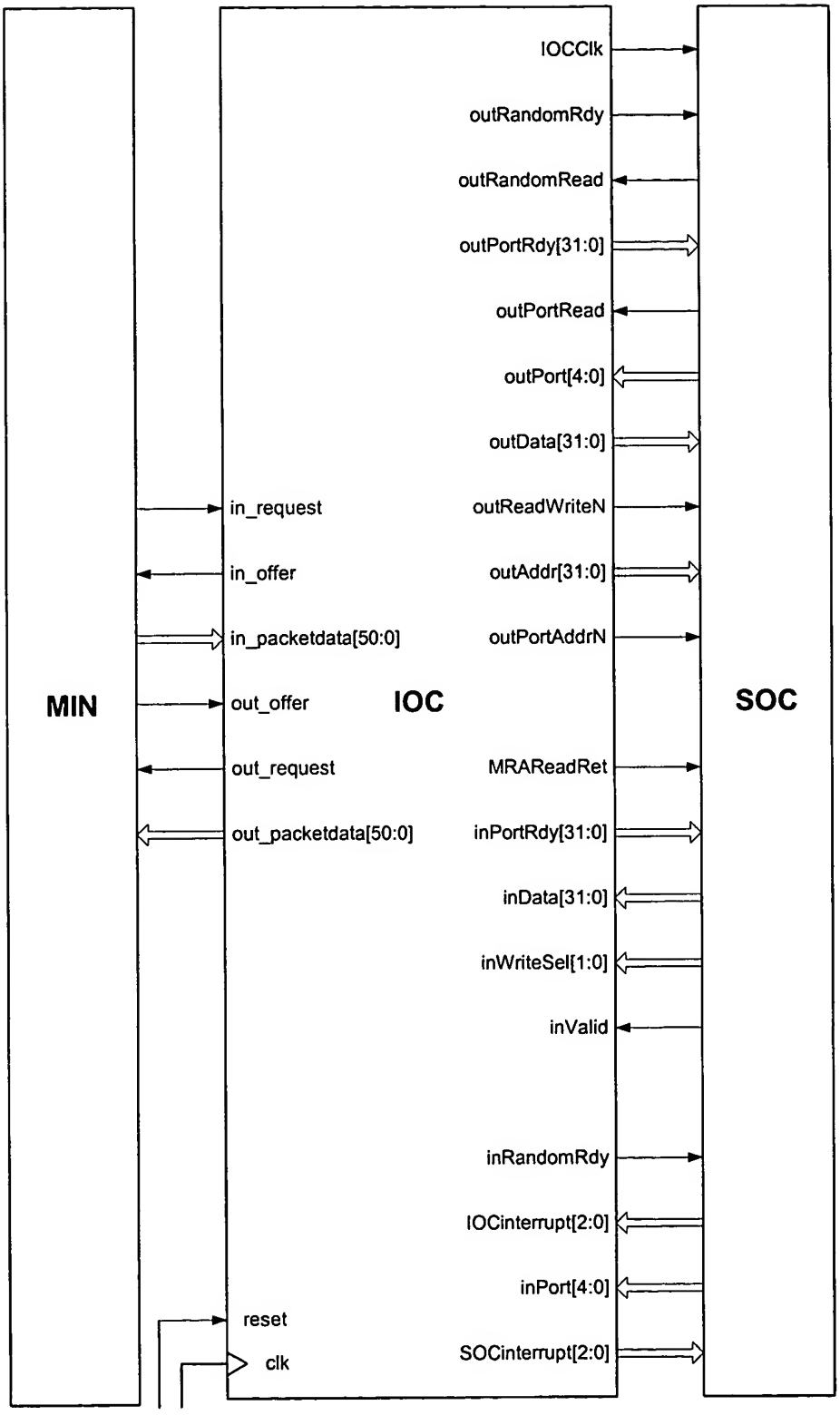
MIN
IOC
SOC
IOCClk
outRandomRdy
outRandomRead
outPortRdy[31:0]
outPortRead
outPort[4:0]
outData[31:0]
outReadWriteN
outAddr[31:0]
outPortAddrN
MRAReadRet
inPortRdy[31:0]
inData[31:0]
inWriteSel[1:0]
inValid
inRandomRdy
IOCinterrupt[2:0]
inPort[4:0]
SOCinterrupt[2:0]
in_request
in_offer
in_packetdata[50:0]
out_offer
out_request
out_packetdata[50:0]
reset
clk

*FIG. 2*

1.

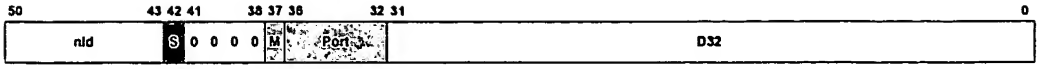


FIG. 3

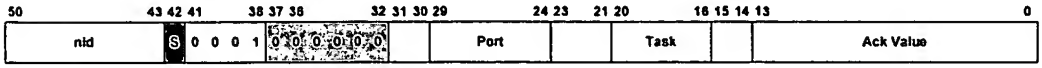


FIG. 4

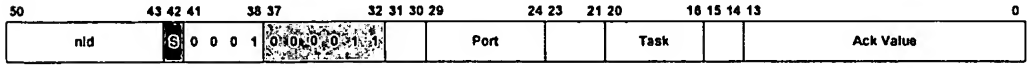


FIG. 5

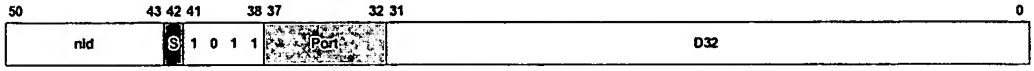


FIG. 6

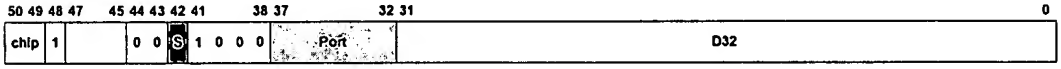


FIG. 7

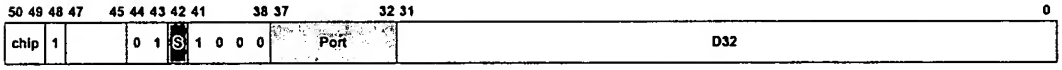


FIG. 8

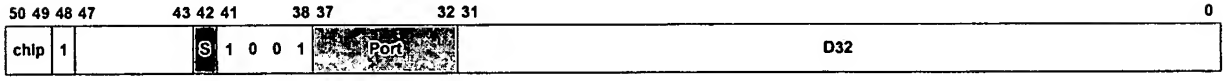


FIG. 9

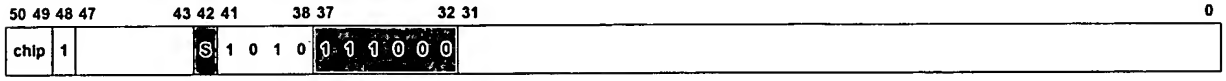


FIG. 10

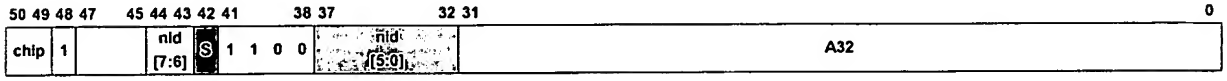


FIG. 11

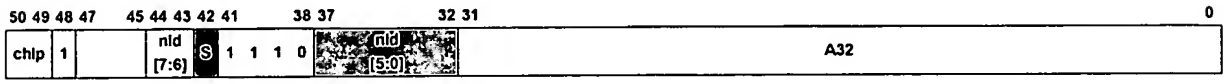


FIG. 12

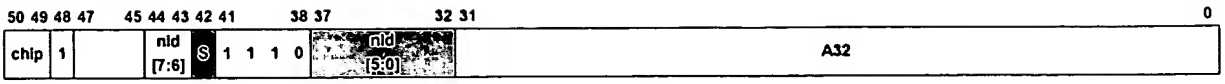


FIG. 13

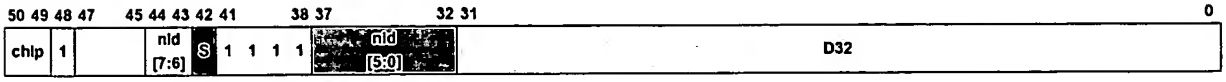


FIG. 14

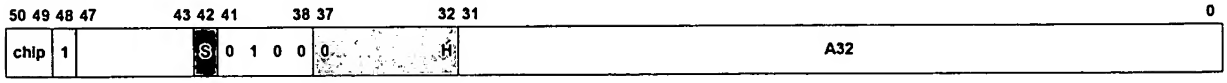


FIG. 15

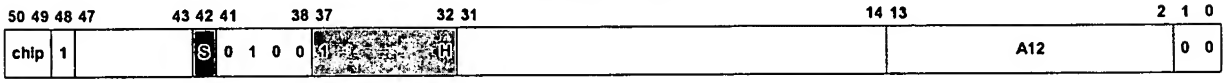


FIG. 16

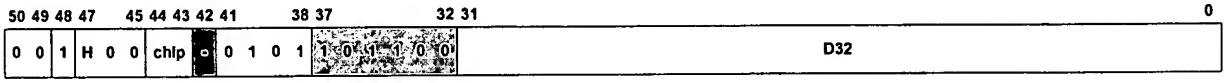


FIG. 17

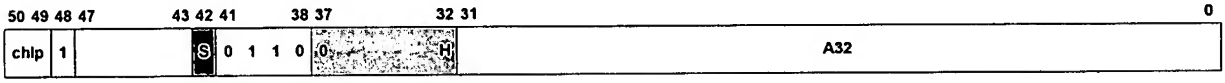


FIG. 18

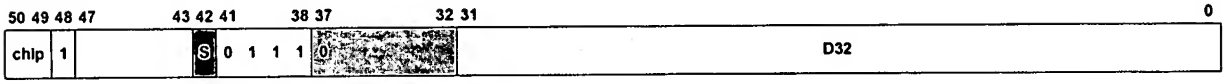


FIG. 19

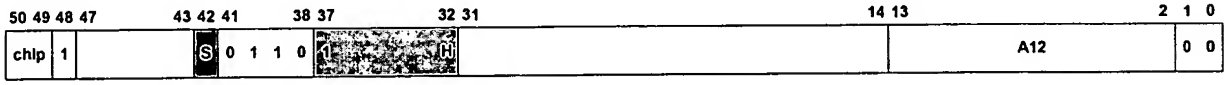


FIG. 20

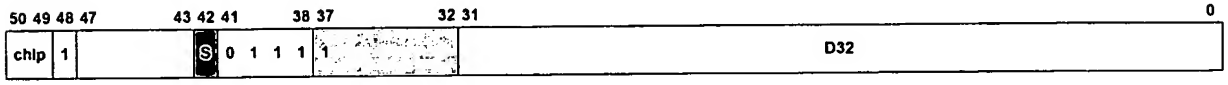


FIG. 21

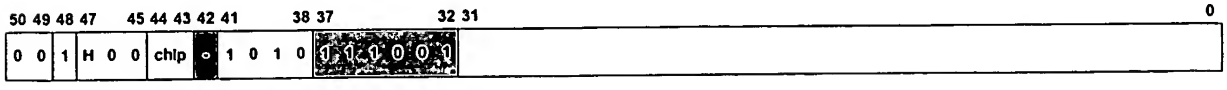


FIG. 22

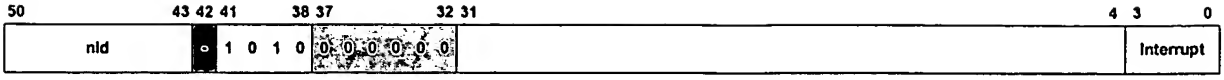


FIG. 23

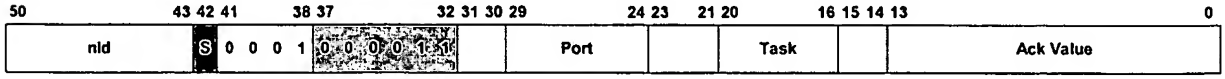


FIG. 24

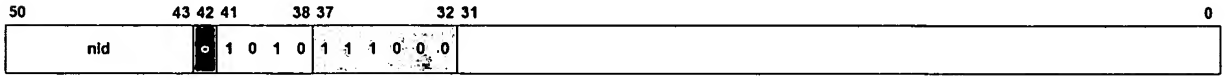


FIG. 25

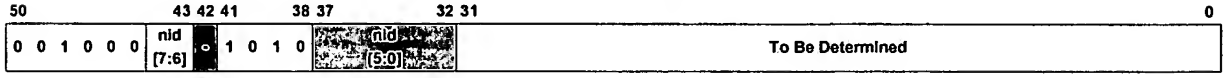


FIG. 26

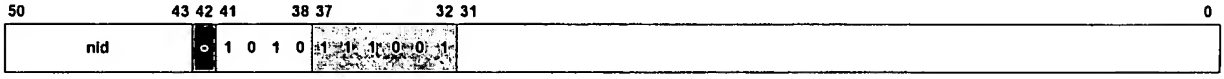


FIG. 27

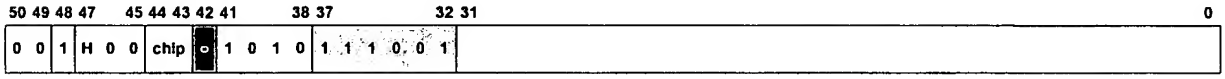


FIG. 28

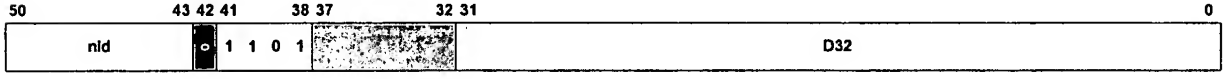


FIG. 29

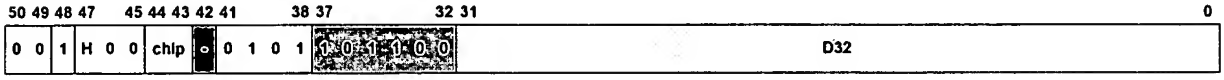


FIG. 30

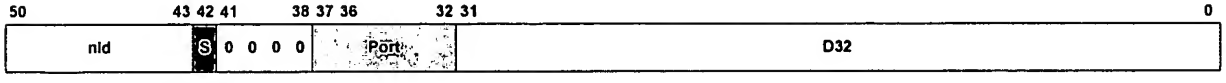


FIG. 31

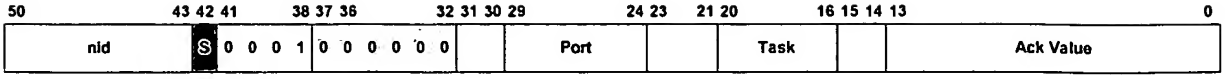


FIG. 32

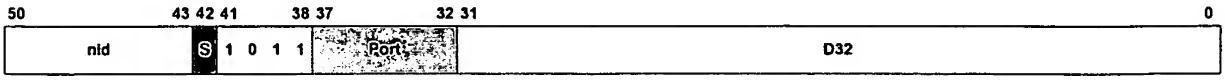


FIG. 33

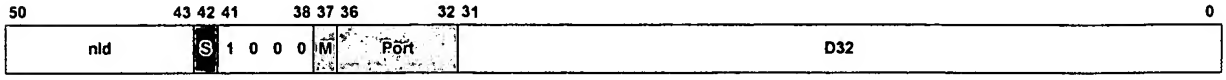


FIG. 34

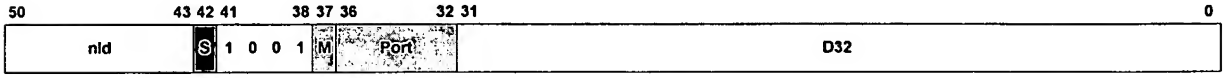


FIG. 35

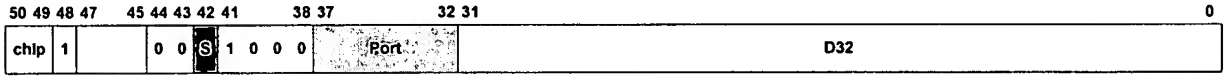


FIG. 36

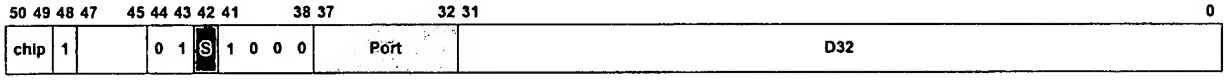


FIG. 37

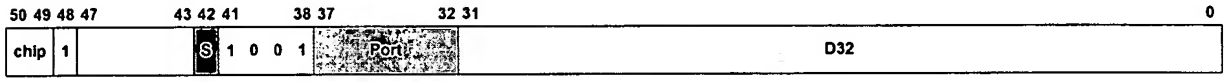


FIG. 38

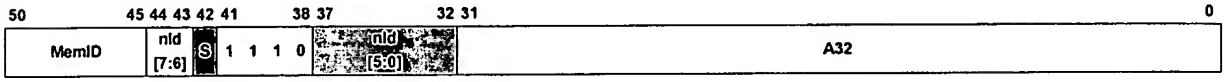


FIG. 39

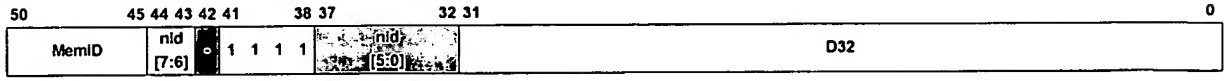


FIG. 40

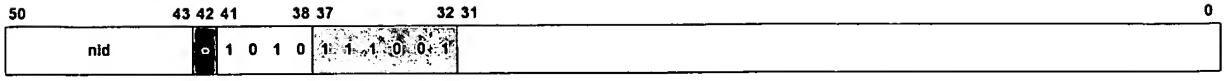


Fig. 41

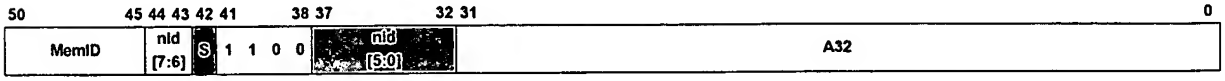


FIG. 42

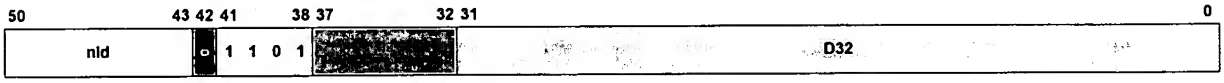


FIG. 43

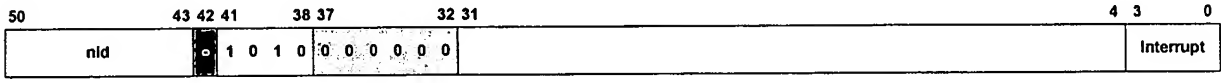


FIG. 44

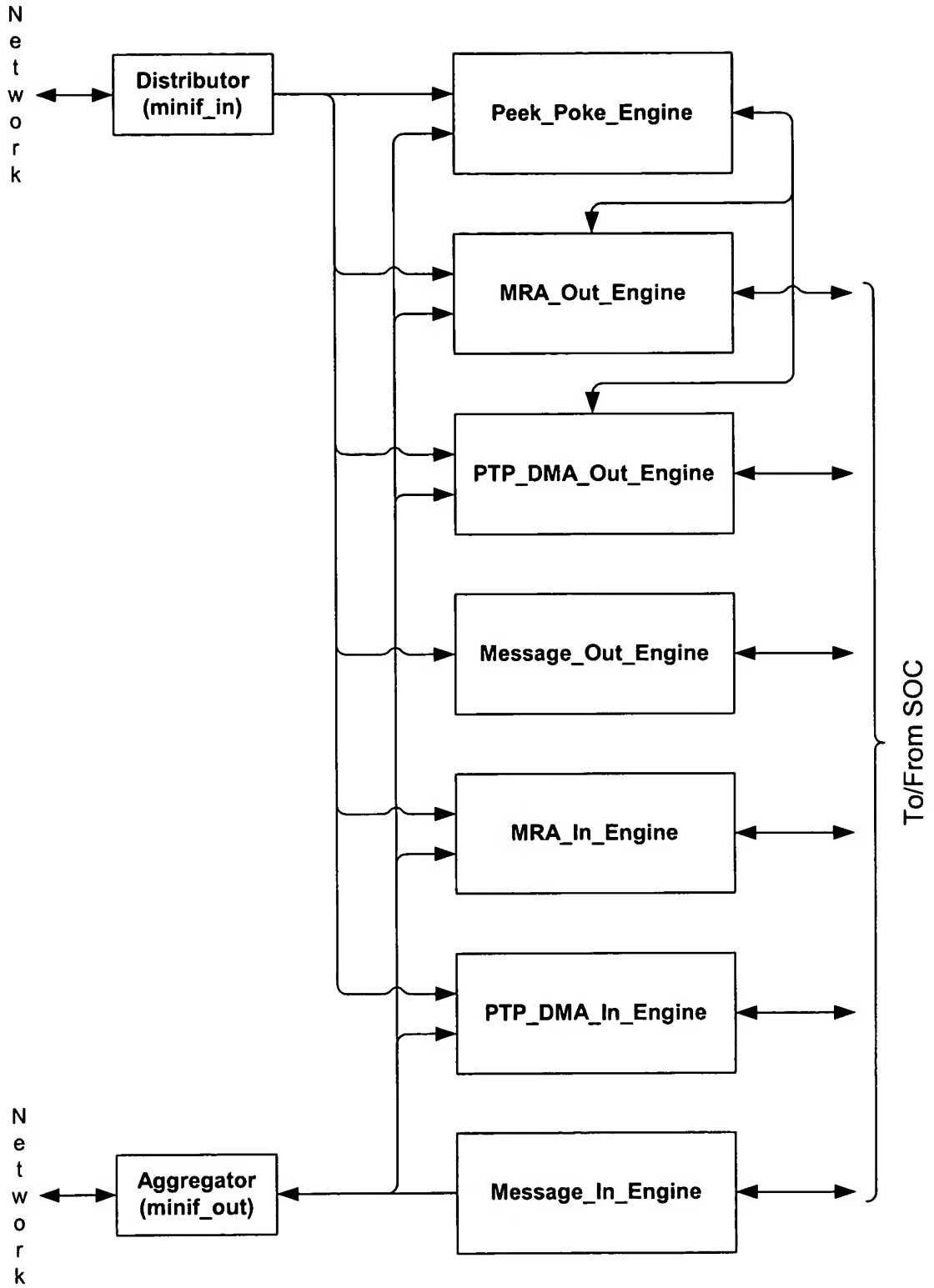


*FIG. 45*

IOC Top Level Block Diagram

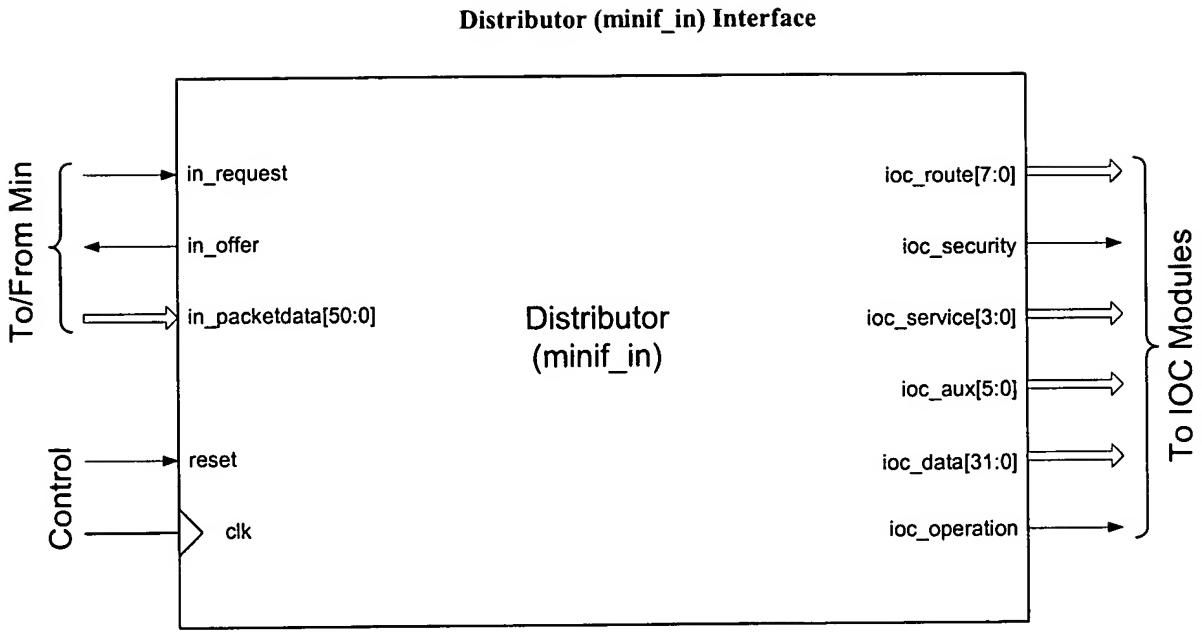
Distributor (minif_in) Interface
To/From Min
in_request
in_offer
in_packetdata[50:0]
Control
reset
clk
Distributor
(minif_in)
ioc_route[7:0]
ioc_security
ioc_service[3:0]
ioc_aux[5:0]
ioc_data[31:0]
ioc_operation
To IOC Modules

*FIG. 46*

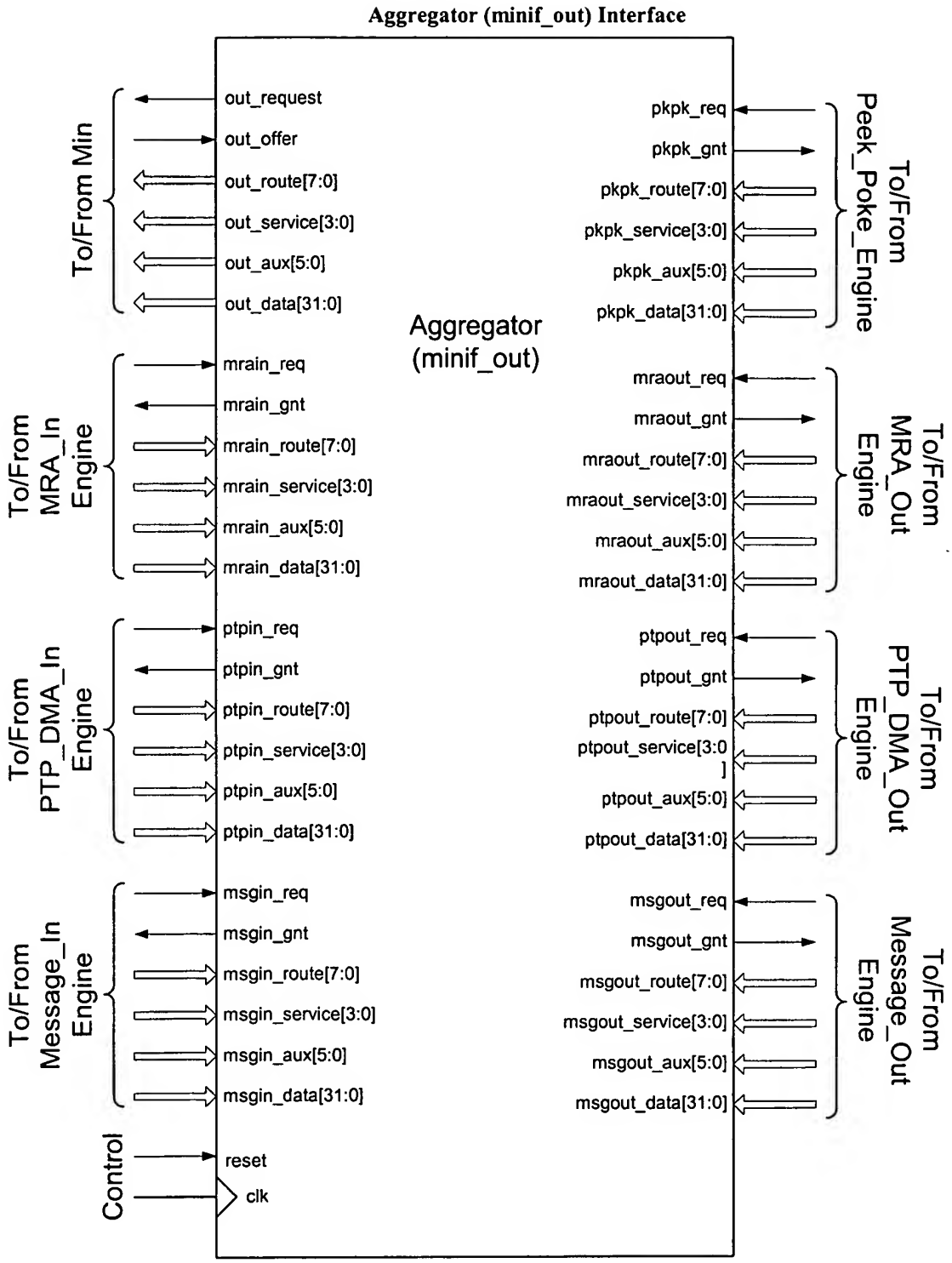
Aggregator (minif_out) Interface
Aggregator (minif_out)
To/From Min
out_request
out_offer
out_route[7:0]
out_service[3:0]
out_aux[5:0]
out_data[31:0]
To/From Peek_Poke_Engine
pkpk_req
pkpk_gnt
pkpk_route[7:0]
pkpk_service[3:0]
pkpk_aux[5:0]
pkpk_data[31:0]
To/From MRA_In Engine
mrain_req
mrain_gnt
mrain_route[7:0]
mrain_service[3:0]
mrain_aux[5:0]
mrain_data[31:0]
To/From MRA_Out Engine
mraout_req
mraout_gnt
mraout_route[7:0]
mraout_service[3:0]
mraout_aux[5:0]
mraout_data[31:0]
To/From PTP_DMA_In Engine
ptpin_req
ptpin_gnt
ptpin_route[7:0]
ptpin_service[3:0]
ptpin_aux[5:0]
ptpin_data[31:0]
To/From PTP_DMA_Out Engine
ptpout_req
ptpout_gnt
ptpout_route[7:0]
ptpout_service[3:0]
ptpout_aux[5:0]
ptpout_data[31:0]
To/From Message_In Engine
msgin_req
msgin_gnt
msgin_route[7:0]
msgin_service[3:0]
msgin_aux[5:0]
msgin_data[31:0]
To/From Message_Out Engine
msgout_req
msgout_gnt
msgout_route[7:0]
msgout_service[3:0]
msgout_aux[5:0]
msgout_data[31:0]
Control
reset
clk

*FIG. 47*

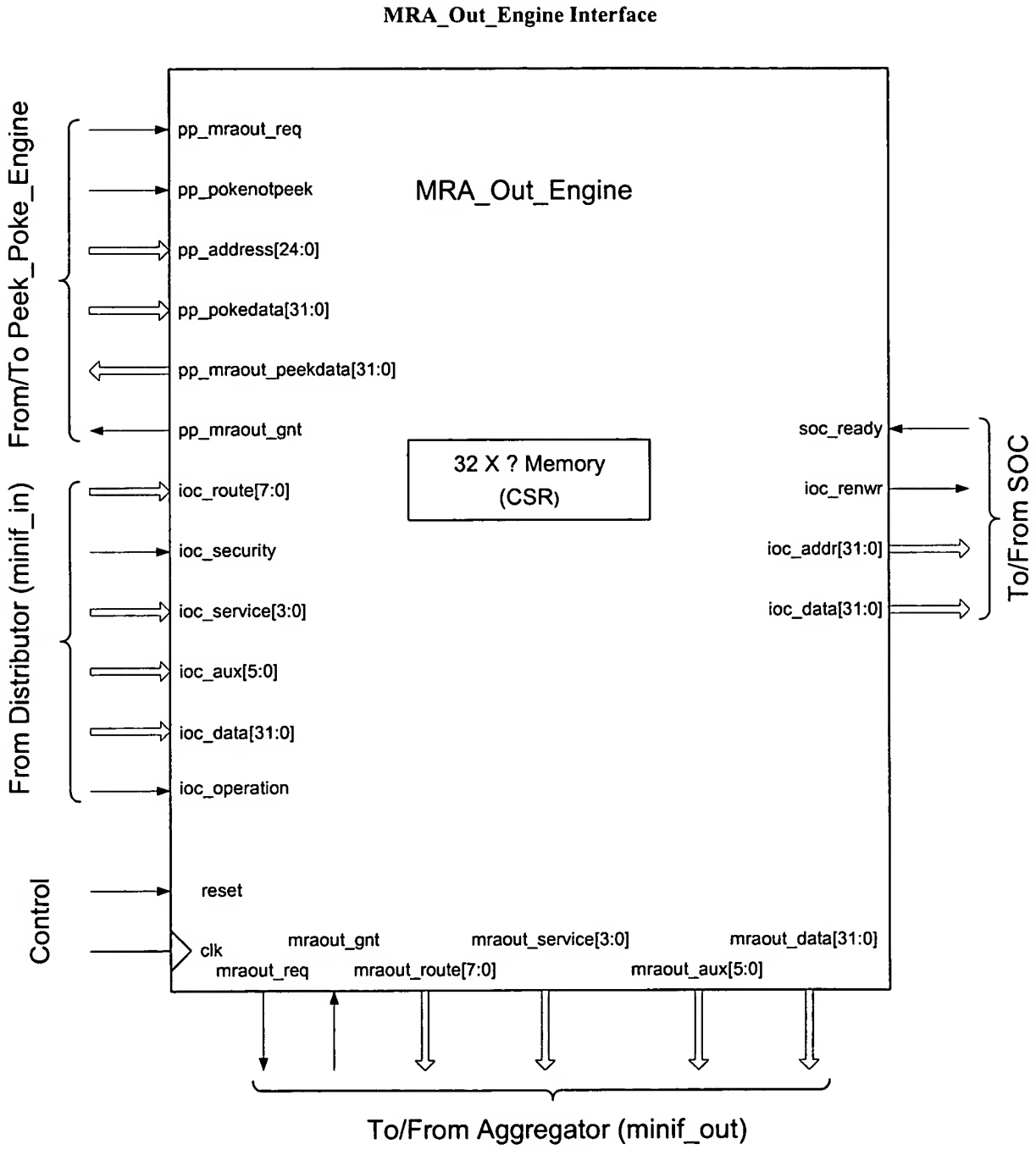
MRA_Out_Engine Interface
MRA_Out_Engine
pp_mraout_req
pp_pokenotpeek
pp_address[24:0]
pp_pokedata[31:0]
pp_mraout_peekdata[31:0]
pp_mraout_gnt
From/To Peek_Poke_Engine
32 X ? Memory
(CSR)
soc_ready
ioc_renwr
ioc_addr[31:0]
ioc_data[31:0]
To/From SOC
ioc_route[7:0]
ioc_security
ioc_service[3:0]
ioc_aux[5:0]
ioc_data[31:0]
ioc_operation
From Distributor (minif_in)
reset
clk
Control
mraout_gnt
mraout_req
mraout_route[7:0]
mraout_service[3:0]
mraout_aux[5:0]
mraout_data[31:0]
To/From Aggregator (minif_out)

*FIG. 48*

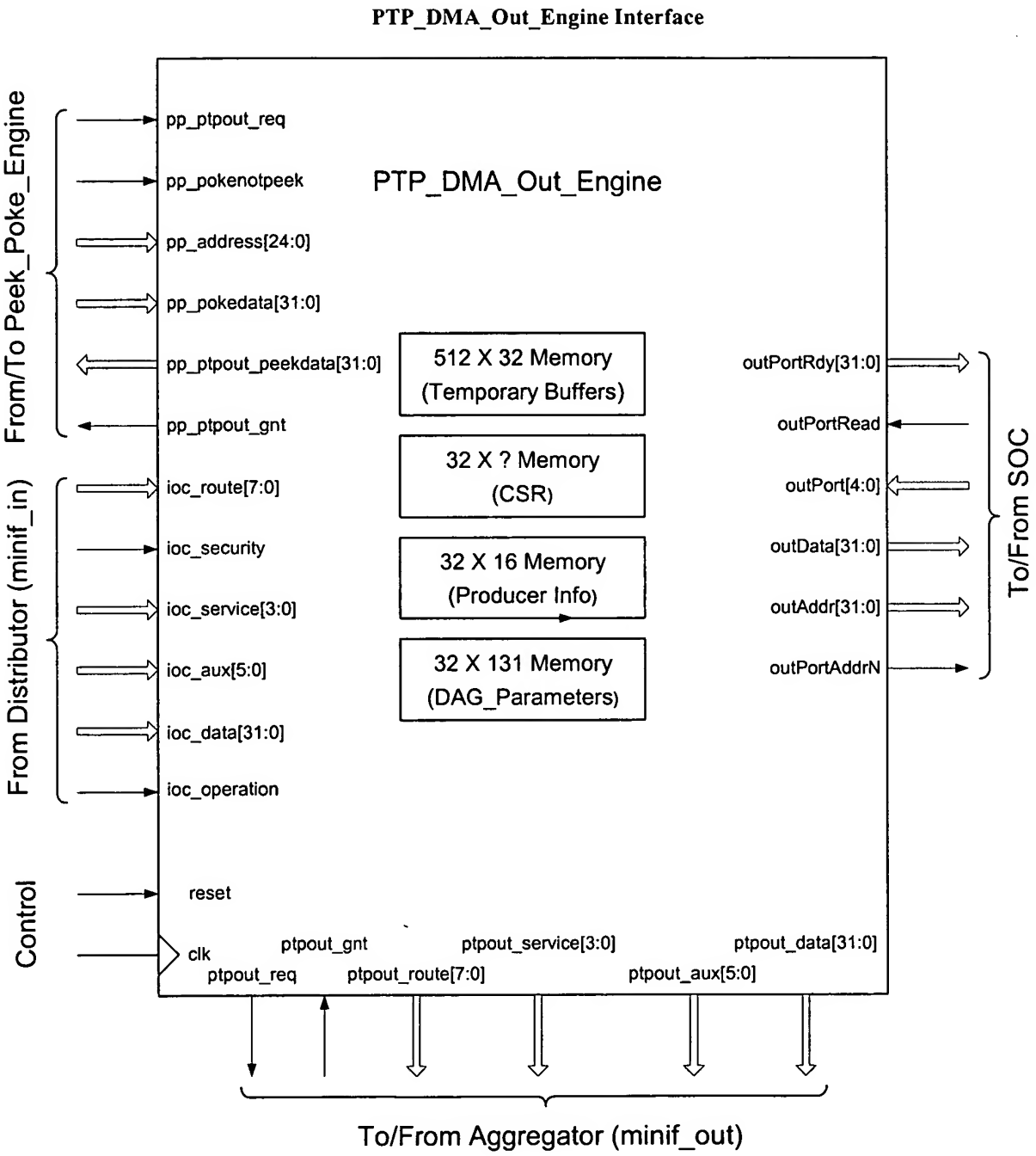
PTP_DMA_Out_Engine Interface
PTP_DMA_Out_Engine
From/To Peek_Poke_Engine
pp_ptpout_req
pp_pokenotpeek
pp_address[24:0]
pp_pokedata[31:0]
pp_ptpout_peekdata[31:0]
pp_ptpout_gnt
From Distributor (minif_in)
ioc_route[7:0]
ioc_security
ioc_service[3:0]
ioc_aux[5:0]
ioc_data[31:0]
ioc_operation
Control
reset
clk
512 X 32 Memory
(Temporary Buffers)
32 X ? Memory
(CSR)
32 X 16 Memory
(Producer Info)
32 X 131 Memory
(DAG_Parameters)
outPortRdy[31:0]
outPortRead
outPort[4:0]
outData[31:0]
outAddr[31:0]
outPortAddrN
To/From SOC
ptpout_gnt
ptpout_service[3:0]
ptpout_data[31:0]
ptpout_req
ptpout_route[7:0]
ptpout_aux[5:0]
To/From Aggregator (minif_out)

*FIG. 49*

. Message_Out_Engine Interface

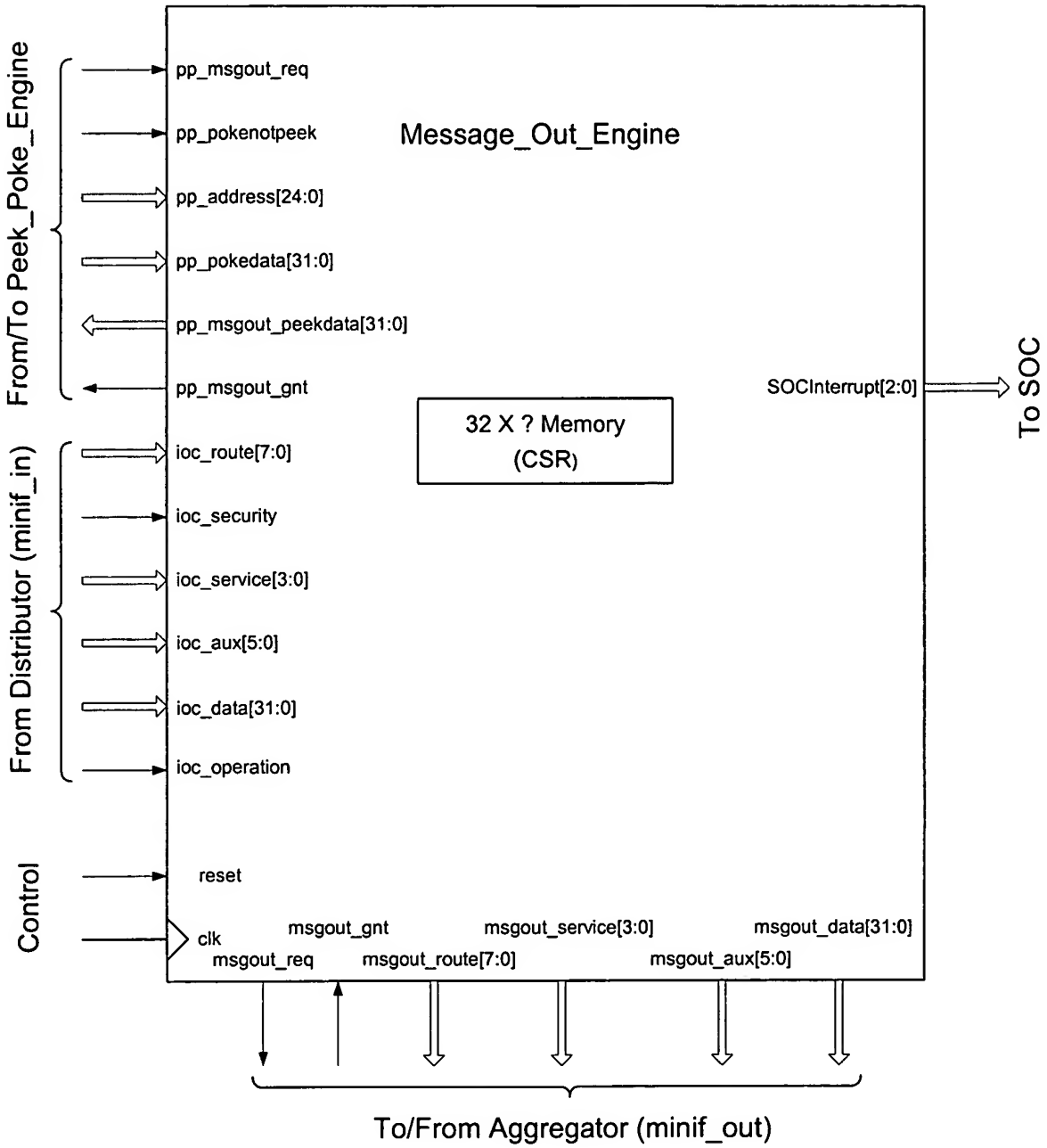


*FIG. 50*

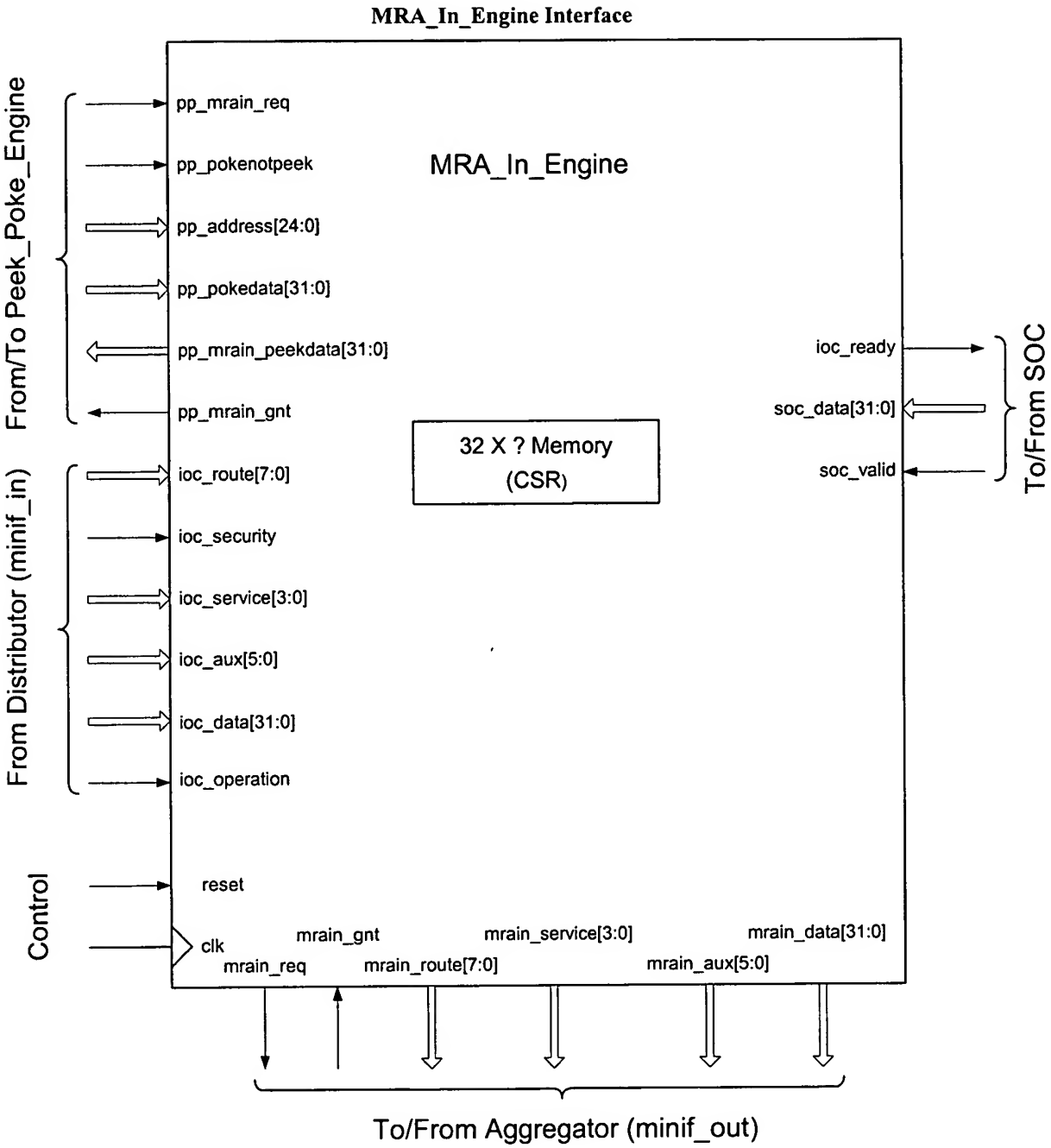
MRA_In_Engine Interface
MRA_In_Engine
From/To Peek_Poke_Engine
pp_mrain_req
pp_pokenotpeek
pp_address[24:0]
pp_pokedata[31:0]
pp_mrain_peekdata[31:0]
pp_mrain_gnt
From Distributor (minif_in)
ioc_route[7:0]
ioc_security
ioc_service[3:0]
ioc_aux[5:0]
ioc_data[31:0]
ioc_operation
Control
reset
clk
32 X ? Memory
(CSR)
ioc_ready
soc_data[31:0]
soc_valid
To/From SOC
mrain_gnt
mrain_service[3:0]
mrain_data[31:0]
mrain_req
mrain_route[7:0]
mrain_aux[5:0]
To/From Aggregator (minif_out)

*Fig. 51*

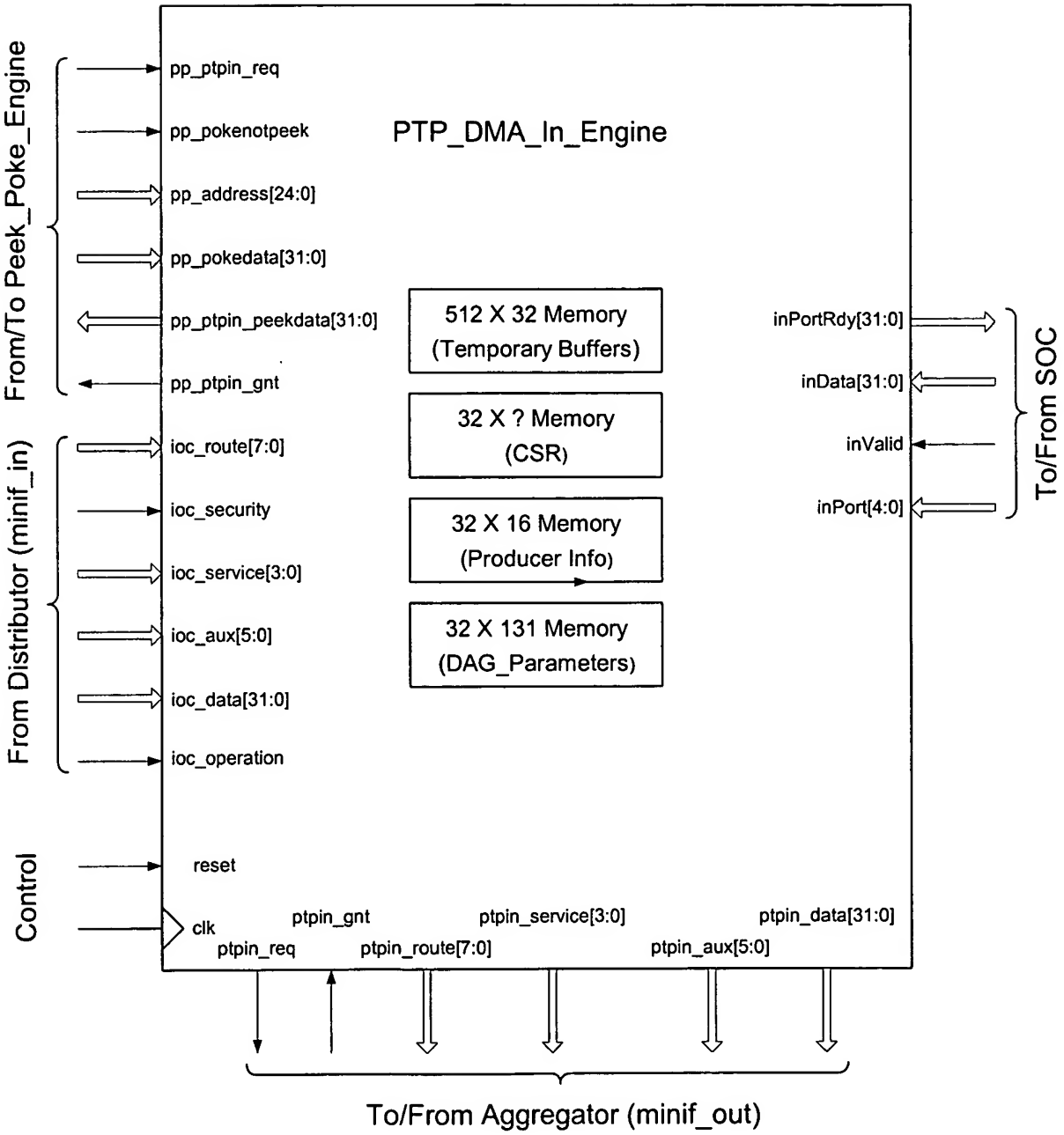
From/To Peek_Poke_Engine
pp_ptpin_req
pp_pokenotpeek
pp_address[24:0]
pp_pokedata[31:0]
pp_ptpin_peekdata[31:0]
pp_ptpin_gnt
PTP_DMA_In_Engine
512 X 32 Memory
(Temporary Buffers)
32 X ? Memory
(CSR)
32 X 16 Memory
(Producer Info)
32 X 131 Memory
(DAG_Parameters)
inPortRdy[31:0]
inData[31:0]
inValid
inPort[4:0]
To/From SOC
From Distributor (minif_in)
ioc_route[7:0]
ioc_security
ioc_service[3:0]
ioc_aux[5:0]
ioc_data[31:0]
ioc_operation
Control
reset
clk
ptpin_gnt
ptpin_service[3:0]
ptpin_data[31:0]
ptpin_req
ptpin_route[7:0]
ptpin_aux[5:0]
To/From Aggregator (minif_out)

*FIG. 52*

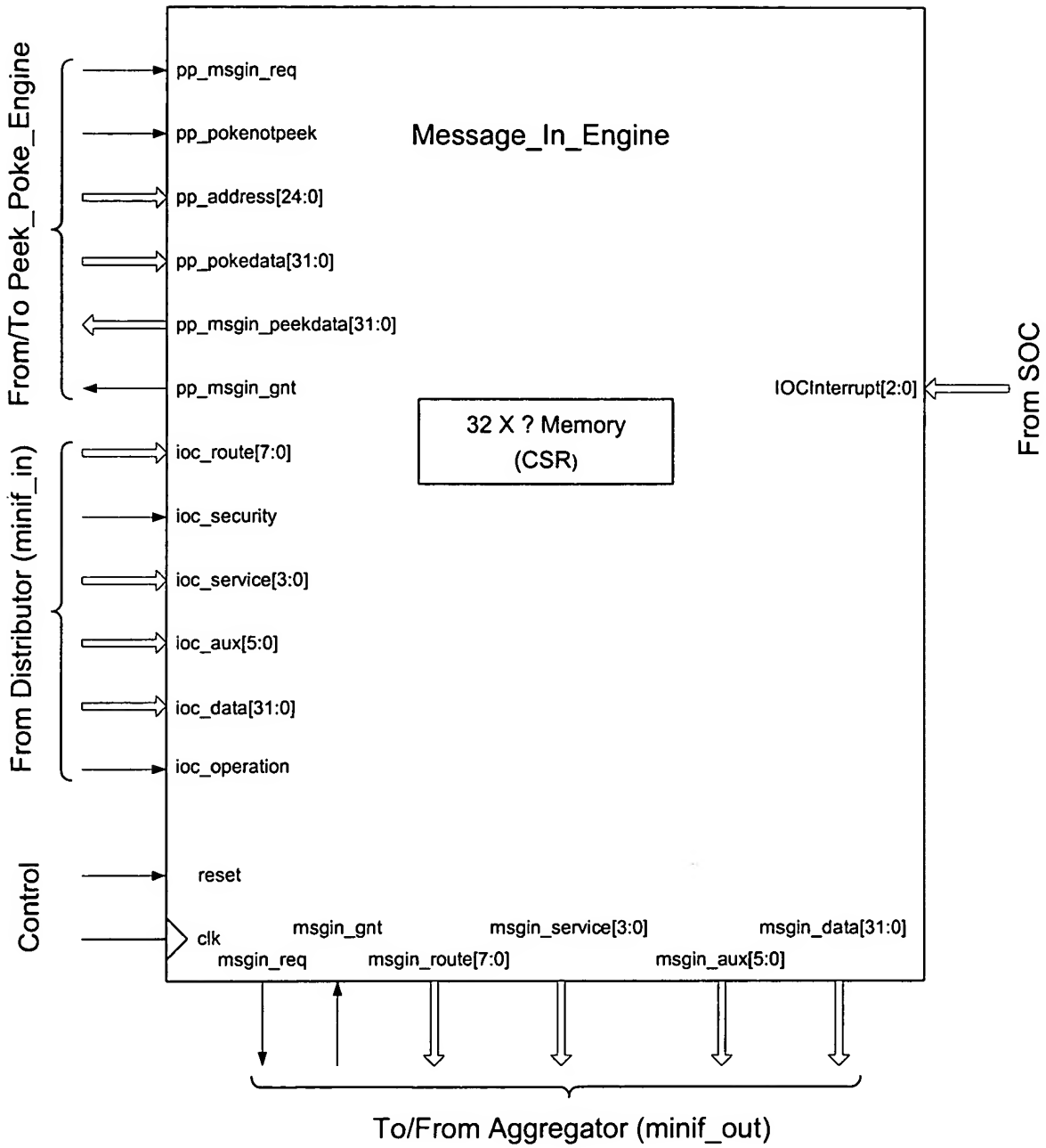
From/To Peek_Poke_Engine
pp_msgin_req
pp_pokenotpeek
pp_address[24:0]
pp_pokedata[31:0]
pp_msgin_peekdata[31:0]
pp_msgin_gnt
Message_In_Engine
32 X ? Memory
(CSR)
IOCInterrupt[2:0]
From SOC
From Distributor (minif_in)
ioc_route[7:0]
ioc_security
ioc_service[3:0]
ioc_aux[5:0]
ioc_data[31:0]
ioc_operation
Control
reset
clk
msgin_gnt
msgin_service[3:0]
msgin_data[31:0]
msgin_req
msgin_route[7:0]
msgin_aux[5:0]
To/From Aggregator (minif_out)

*FIG. 53*

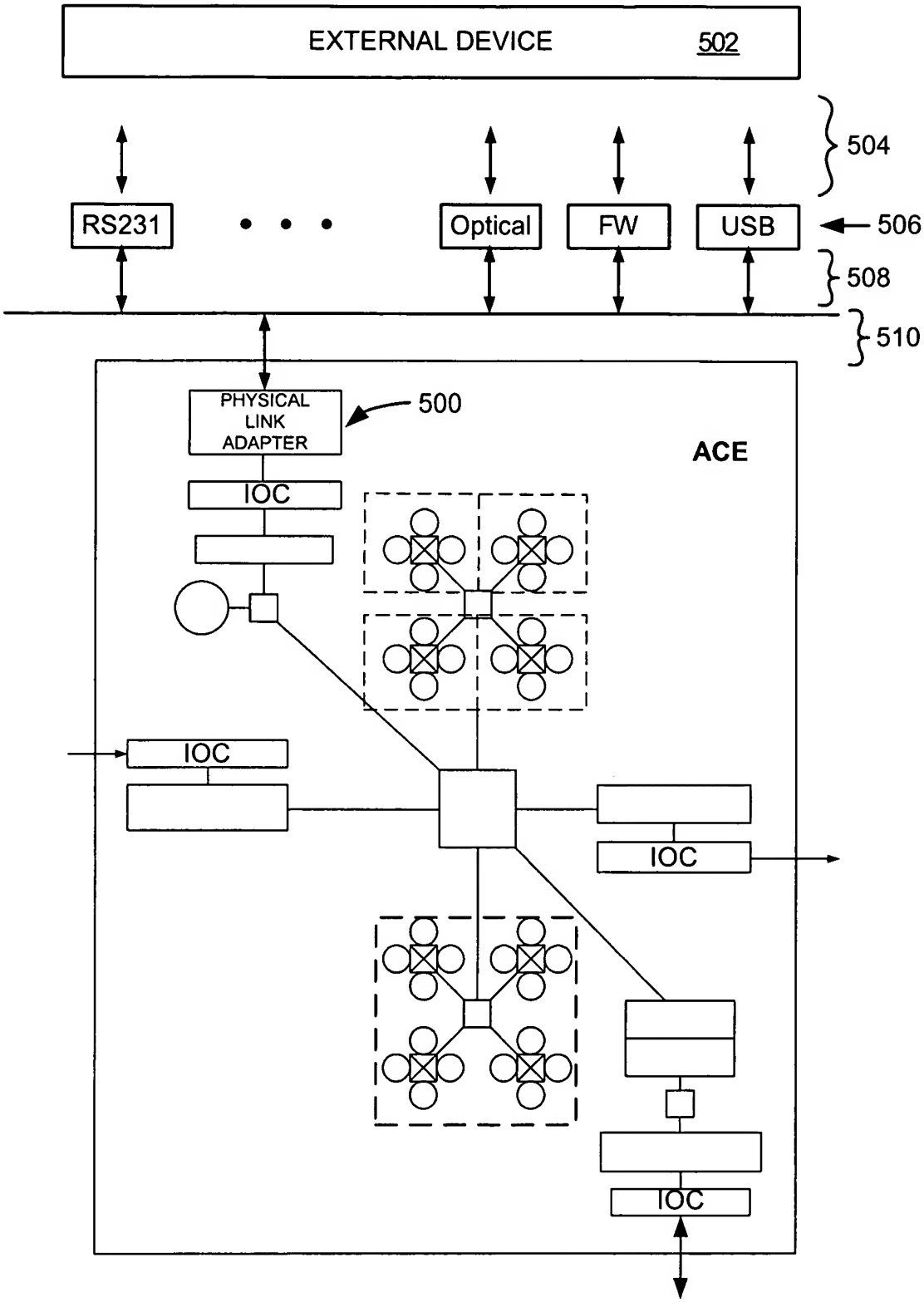
EXTERNAL DEVICE
502
504
RS231
Optical
FW
USB
506
508
510
PHYSICAL LINK ADAPTER
500
ACE
IOC
IOC
IOC
IOC

*FIG. 54*

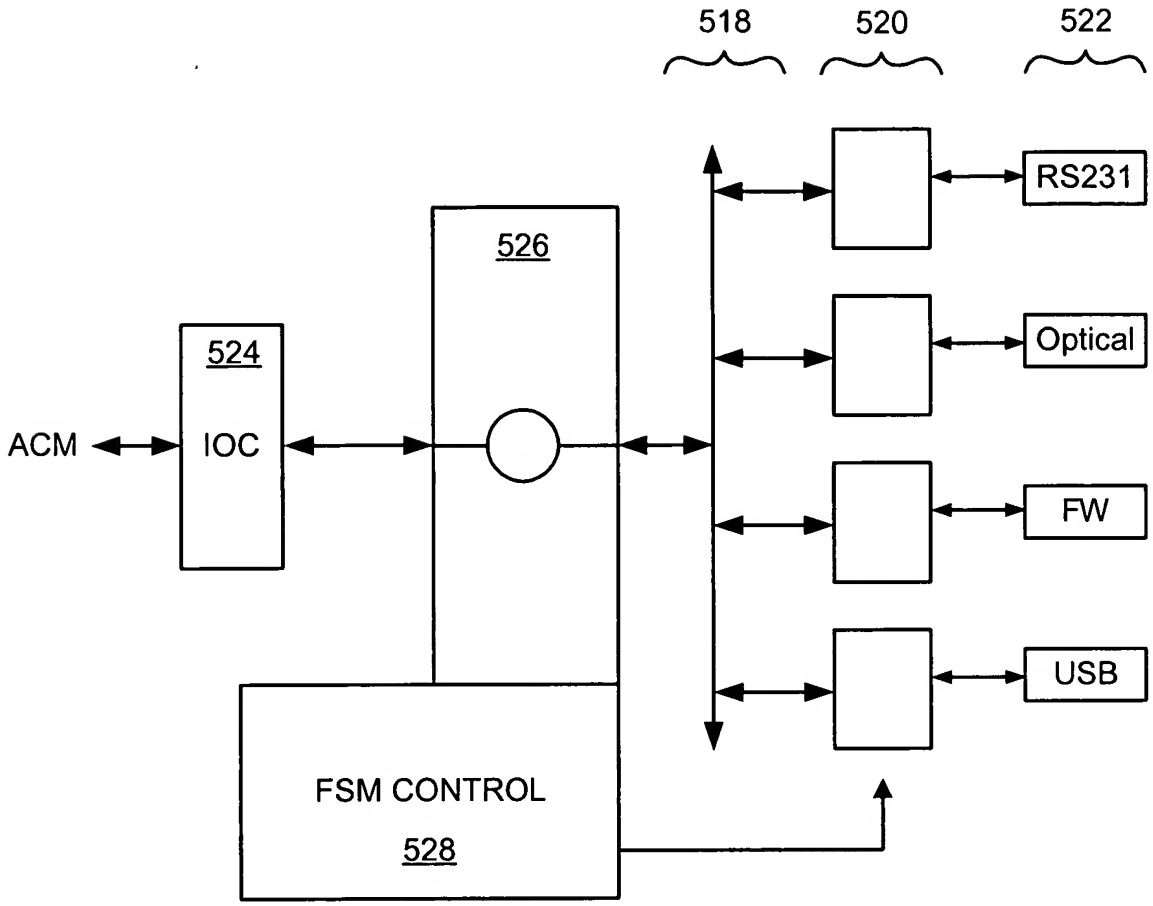
518
520
522
RS231
Optical
FW
USB
526
524
ACM
IOC
FSM CONTROL
528

*FIG. 55*